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IN THE SPECIFICATION:

The replacement abstract and replacement paragraph are submitted to address some of the Examiner's concerns identified in the September 7, 2006 Office Action. Applicants submit that no new matter is injected into the application by way of the substitute abstract and paragraph.

Please replace the abstract with the following substitute abstract:

~~Viterbi decoder~~

Viterbi decoder for decoding a received sequence of data symbols which are coded using a predetermined coding instruction is provided. ~~, having: (a)~~ The Viterbi decoder includes a branch metric calculation circuit ~~(5)~~ for calculation of branch metrics ~~(λ)~~ for the received sequence of coded data symbols[[;]] . The Viterbi decoder includes ~~(b)~~ a path metric calculation circuit ~~(9)~~ for calculation of path metrics ~~(γ)~~ as a function of the branch metrics ~~(λ)~~ and the coding instruction, with the calculated path metrics in each case being compared with an adjustable decision threshold value ~~(SW)~~ in order to produce an associated logic validity value~~; and having~~. The Viterbi decoder also includes ~~(c)~~ a selection circuit ~~(20)~~ which temporarily stores those path metrics whose validity value is logic high in a memory, and selects from the temporarily stored path metrics that path with the optimum path metric.

~~Figure 6~~

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Please replace the paragraph beginning at page 1, line 9, with the following paragraph:

A Viterbi decoder is known from Tsui Chi-Ying, et al. "Low Power ACS Unit Design for the Viterbi Decoder" in IEEE Proceedings of the 1998 International Symposium on Circuits and Systems, ISCAS 1999, pages 137-140 Volume 1, which contains a branch metric calculation circuit for calculation of branch metrics, a path metric calculation circuit for calculation of path metrics as a function of the branch metrics, and a selection circuit, in order that ~~that~~ the path which has the optimum path metric is selected from the temporarily stored path metrics.